APPLICATION

FOR

UNITED STATES LETTERS PATENT

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TITLE: SOLDER INTERCONNECT TECHNIQUES

DOCKET NO. EN999048D

INTERNATIONAL BUSINESS MACHINES CORPORATION

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SOLDER INTERCONNECT TECHNIQUES

Field of the Invention:

The present invention relates to soldering techniques and, more particularly, to a solder method that enhances solder interconnects by eliminating solder joint failures caused by micro-cracking at or near the solder intermetallic interface.

BACKGROUND OF THE INVENTION

The fatigue life of solder interconnects is often poor, because cracks develop near an intermetallic layer. The damaging process is due to the build-up of inelastic deformation (creep) that leads to cavity nucleation, growth, and coalescence along grain boundaries. The increasing damage tends to produce micro-cracks at the boundaries. These boundary micro-cracks are disposed roughly normal to the direction of maximum tensile stress.

The factors that influence the aforementioned damage include: (a) the shape of the joint, which influences the stress concentration at the free joint boundaries; (b) the build-up of intermetallics, which are known to locally increase stress in solder at and above the intermetallic layer; and (c) the local coefficient of thermal expansion (CTE) mismatch between the pad and the solder.

It is also observed that dissolved copper, gold, or other metallic pad coating materials locally contaminate solder. The contaminants increase the solder brittleness, making the solder susceptible to micro-cracking, when compared with bulk behavior.

The present invention seeks to increase the fatigue life of the solder joint, by limiting the damage caused by micro-cracking in the solder joint. This objective is achieved by redistributing the stresses in solder, thus constraining the cracks. Such containment can be accomplished by creating obstacles along the crack path, redirecting the crack away from the intermetallic layer, or by increasing the path length along which the crack is to propagate. The solder layer can be designed to include a serpentine, interrupted, or interdigitated boundary. The

method can be applied to ball grid arrays, column grid arrays, surface mount technology (SMT) joints, etc.

Discussion of Related Art:

In United States Patent No. 5,242,569, issued to Kang et al, on September 7, 1993, for THERMOCOMPRESSION BONDING IN INTEGRATED CIRCUIT PACKAGING, a thermocompression bonding method is described that allows bonding to be achieved at lower temperatures. The process produces a soft, deformable layer of metal that is free of dendritic protrusions.

In United States Patent No. 5,172,473, issued to Burns et al, on December 22, 1992, for METHOD OF MAKING CONE ELECTRICAL CONTACT, a method of achieving improved electrical contact is illustrated. Contact is improved by generating cone-shaped projections upon a mating surface. The cones enhance ohmic contact by intermeshing and wiping.

In United States Patent No. 5,118,299, issued to Burns et al, on June 2, 1992, for CONE ELECTRICAL CONTACT, an electrical interconnection is shown featuring two detachable surfaces having intermeshing cone projections. The cones

enhance ohmic contract by intermeshing and wiping.

In United States Patent No. 3,881,799, issued on May 6, 1975, to Elliott et al, for RESILIENT MULTI-MICRO POINT METALLIC JUNCTION, a dynamic interfacing contact device is disclosed. The device provides multiple points of contact between opposing parallel surfaces of a pair of conductors. The points of contact are provided by a number of spaced-apart, metal protrusions.

In United States Patent No. 4,751,563, issued to the common assignee, a microminiaturized electrical interconnection device is described. Electrical connection on a first pad is tangentially raised at about sixty degrees and brought into intimate contact with a second metallic layer.

SUMMARY OF THE INVENTION

In accordance with the present invention, there is provided a method and article of fabrication, featuring a solder layer that comprises a serpentine, interrupted, or interdigitated boundary. The non-planar design of the

boundary layer increases the fatigue life of the solder joint, by limiting the damage caused by micro-cracking. This irregularity of the solder boundary constrains the propagation of cracks by creating obstacles along the crack path, redirecting the crack away from the intermetallic layer, or by increasing the path length along which the crack propagates.

It is an object of this invention to provide a method and article of fabrication that improves the fatigue life of solder joints.

It is another object of the invention to produce a solder joint that constrains cracking along the intermetallic boundary.

BRIEF DESCRIPTION OF THE DRAWINGS

A complete understanding of the present invention may be obtained by reference to the accompanying drawings, when considered in conjunction with the subsequent detailed description, in which:

FIGURE 1 illustrates a plan view of a prior art configuration of a length of solder disposed at an intermetallic surface;

FIGURE 2 depicts a plan view of the micro-crack propagation at the solder boundary layer, using the solder configuration of FIGURE 1;

FIGURE 2a is a greatly enlarged photograph of actual solder pads with defects represented in FIGURE 2;

FIGURES 3a through 3g show a plan view of seven embodiments of the pad configuration of this invention; and

FIGURE 4 illustrates a plan view of the micro-crack propagation at the solder boundary layer, using the pad configuration of FIGURE 3a.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Generally speaking, the invention features a method as well as solder pad configurations which increase the fatigue life of the solder joint. The method and pad configurations

reduce the damage which is normally caused by micro-cracking at the solder and near intermetallic interface. This non-planarity of the pad surface constrains the propagation of cracks by creating obstacles along the crack path, redirecting the crack away from the intermetallic layer, or by increasing the path along which the crack propagates.

Now referring to FIGURE 1, a plan view of a prior art metallic pad 10 is illustrated. The straight edge 12 of the solder boundary induces micro-cracking 14 in solder near the intermetallic layer, as shown in FIGURE 2. The micro-crack 14 tends to propogate, because there is no constraint against its growth.

Referring to FIGURES 3a through 3g, a plan view of a plurality of non-planar shaped strips of pad 16, 17, 18, 19, 21, 22, and 23 respectively, is depicted. FIGURE 3a depicts an undulating or serpentine strip of pad 16; FIGURE 3b shows an undulating or serpentine strip of pad 17 having a straight base strip 17a; FIGURE 3c illustrates an interdigitated strip of pad 18; FIGURE 3d depicts a strip of pad 19 having a curved, central digit 19a; FIGURE 3e depicts a pad having raised, concentric walls 21a and 21b, FIGURE 3f shows a pad 22 having a raised cross-shaped feature 22a; and

FIGURE 3g illustrates a pad 23 having a plurality of foreshortened substantially cylindrical protrusions 23a disposed perpendicularly with respect to the major plane of the pad 23.

Referring to FIGURE 4, a solder joint at the intermetallic boundary is shown, using the serpentine solder configuration depicted in FIGURE 3a. It will be observed that the respective micro-cracking 20 at each intermetallic boundary is following a circuitous or meandering path. The lengthening of the crack pathway increases the useful life of the solder joint. Other pad configurations are shown in FIGURES 3b through 3d. As before, this results in micro-crack pathways which are interrupted, lengthened, or constrained. In similar manner, these configurations are expected to increase fatigue life of the solder joint, as is that of the solder design shown in FIGURE 3a.

Since other modifications and changes varied to fit particular operating requirements and environments will be apparent to those skilled in the art, the invention is not considered limited to the examples chosen for the purpose of disclosure, and covers all changes and modifications which do not constitute departures from the true spirit and scope

of this invention.

Having thus described the invention, what is desired to be protected by Letters Patent is presented in the subsequently appended claims.